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IV B.Tech II Semester(R07) Regular Examinations, April 2011 DIGITAL DESIGN THROUGH VERILOG (Common to Electronics & Communication Engineering, Electronics & Computer

Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE questions All questions carry equal marks ****

- 1. (a) Explain NAND Gate primitive with verilog module.
 - (b) Explain NOR Gate primitive with verilog module.
- 2. (a) Classify and explain strengths & contention resolution.
 - (b) Design a module to illustrate use of the wand type net and test bench with simulation results.

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- 3. Write a short notes on:
 - (a) Functional Bifurcation
 - (b) Intra Assignment delays.
- 4. (a) Explain a Dice game with Block diagram.
 - (b) Explain a Dice game using flow chart.
- 5. (a) Design CMOS switch with a single control line.
 - (b) Design a code, test bench, results for a CMOS switch with a single control line.

6. Explain about:

- (a) Display tasks.
- (b) Strobe tasks.
- (c) Monitor tasks with examples.
- 7. (a) Write the Difference between CPLD & FPGA
 - (b) Explain about logic array block.
- 8. (a) Explain 6116 static RAM with block diagram.
 - (b) Explain Read cycle timing of SRAM.

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- 1. Write a short notes on:
 - (a) Concurrency
 - (b) Functional verification.
- 2. Draw the half adder circuits interms of Ex-OR & AND gates. Prepare the Half adder module and test bench in terms of EX-OR and AND gate primitives.
- 3. (a) Explain about forever Loop.
 - (b) Write the differences between Begin-end and Fork-join blocks with examples.
- 4. (a) Write a module and test Bench for BCD adder.
 - (b) Draw the synthesized circuit and results of test Bench for BCD adder.
- 5. (a) Explain about module paths.
 - (b) Design a verilog modules using path delays.
- 6. (a) Draw the block diagram for a divider that divides an 8-bit dividend by a 5-bit divisor to give a 3bit quotient. The Dividend register should be loaded when St=1.
 - (b) Draw an SM chart for control unit.
- 7. (a) Write the Difference between CPLD & FPGA.
 - (b) Explain about logic array block.
- 8. Design HDL Module ALU operations for register memory instructions.



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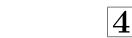
Answer any FIVE questions All questions carry equal marks ****

- 1. Explain different levels of design descriptions in verilog.
- 2. (a) Design a Module and test bench for a fulladder.
 - (b) Draw the synthesized output of full adder.
- 3. Write short notes on:
 - (a) Functional Bifurcation.
 - (b) Wait construct with example.
- 4. Write short notes on:
 - (a) Bidirectional gates.
 - (b) Time delays with switch primitives.
- 5. What do you meant by user defined primitives (UDP) and explain the types with examples.

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- 6. (a) Draw the block diagram for a divider that divides an 8-bit dividend by a 5-bit divisor to give a 3 bit quoetient the dividend register should be loaded when St=1.
 - (b) Draw a SM chart for control unit.
- 7. Explain about XC4000 series CLB with Block Diagram.
- 8. (a) Explain 6116 static RAM with block diagram.
 - (b) Explain Read cycle timing for SRAM.

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- (a) What are the system tasks available in verilog. 1.
 - (b) Explain about Data types in verilog.
- (a) Design a RS flip flop with NAND gates. 2.
 - (b) Write an verilog code for RS flip flop with NAND Gates.
- (a) Draw the flow chart for simulation flow. 3.
 - (b) Explain about disable construct with example.
- 4. Write a short notes on:
 - (a) Binary operators.
 - (b) Ternary operators.
 - (c) Arithmatic operators.
 - (d) Bit wise logical operators.
- on ter 5. What is FSM ? Explain the types in FSM with the help of Block diagram.
- (a) Explain a Dice game with block diagram. 6.
 - (b) Explain a Dice game using Flow chart.
- 7. Explain about XC4000. Series CLB with block diagram.
- 8. (a) Explain about simplified 486 Bus model.
 - (b) Explain about UART design.

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